PCI 9054

Design Notes Rev. 1.8
July 2003

Design Notes Documentation

A. Affected Silicon Revision

This document details Design Notes for the following silicon:

Product	Revision	Description	Status
PCI 9054AB	PCI9054-AB50PI	Released 176-pin PQFP Product	August 1999
PCI 9054AB	PCI9054-AB50BI	Released 225-pin PBGA Product	August 1999
PCI 9054AC	PCI9054-AC50PI	Released 176-pin PQFP Product	January 2002
PCI 9054AC	PCI9054-AC50BI	Released 225-pin PBGA Product	January 2002

B. Documentation Revision

The following documentation is the baseline functional description of the silicon.

Document	Revision	Description	Publication Date
PCI 9054 Data Book	2.1	Released Data Book	January 2000

C. Design Notes Summary:

#	Description
1	Direct Slave Local Bus Continuous Burst in M-Mode
2	Local Interrupt (LINT#) Input/Output
3	Delayed Read Mode Bit (MARBR[24])
4	EEPROM Serial Read Feature (CNTRL[27])
5	BDIP# Pin
6	Operation of PCI 9054 Buffers in 3.3 Volt Signaling Environment
7	Local Parity Error Status Bit and Interrupt Assertion
8	Hot Swap Register Accesses from Local Bus (Applies to revision AB only; fixed in AC silicon)
9	Retried Direct Slave Single Read completed as Burst Read
10	Multiplexed output pin DMPAF (Direct Master Programmable Almost Full) negation or MDREQ# (M-Mode IDMA Request) assertion timing
11	EEDI/EEDO pull-up/pull-down documentation
12	PCI 9054AB will occasionally drive LSERR# output in Test mode (Applies to revision AB only; fixed in AC silicon)
13	PCI Target Abort during DMA Transfer
14	Interrupt Control/Status register indication of a Master or Target Abort
15	PCI Power Management Interface Specification version support
16	Capability Pointers values must be either default value or 0
17	Direct Slave Transfer Size
18	VPD Implementation

D. Design Notes for Revisions AB and AC

1. Direct Slave Local Bus Continuous Burst in M-Mode

Design Issue: During continuous burst with PCI-to-Local Direct Slave Write transaction(s) in M-Mode, if the PCI Byte Enables (C/BE[3:0]#) are not all 0 (enabled) during a data phase:

- If the PCI address of that data is paragraph-aligned (16-byte boundary, address x0h), then the PCI 9054 will perform single cycles on the Local bus up to the next 16-byte boundary, toggling TSIZ[0:1] according to the PCI Byte Enable values and issuing TS#, for each Local bus address. Bursting will resume at the next paragraph boundary if all PCI Byte Enables are asserted for that address.
- If the PCI address of that data is x4h, x8h or xCh then the PCI 9054 will continue the burst and pass all bytes to the Local bus, keeping TSIZ[0:1] at the constant value of 0 regardless of the value of the PCI Byte Enables.

Recommendation: During a PCI-to-Local Direct Slave write burst transaction(s), C/BE# toggle should occur on the paragraph-aligned address, or keep all bytes enabled.

2. Local Interrupt (LINT#) Input/Output

Design Issue: Customers who are considering migrating from previous generation PLX Bus Masters to the PCI 9054, and have developed software for previous generation devices, might experience some difficulty with the Local Interrupt. Unlike previous PLX products, the PCI 9054 has multiplexed LINTi# and LINTo# as a single pin (LINT#).

Recommendation: Whenever LINTo# is driven low, the input feedback of the internal I/O buffer causes PCI INTA# to be driven low. To disable the PCI INTA# assertion, the LINTi# enable bit INTCSR [11] needs to be disabled, ‘0’. The default value of INTCSR [11] after PCI reset is ‘0’.
Whenever a PCI interrupt INTA# needs to be generated via the LINTi# pin, the enable bit INTCSR [11] needs to be enabled, ‘1’.

3. Delayed Read Mode bit (MARBR[24])

Changes to PCI 9054 Data Book revision 2.1: The name for the Mode/DMA Arbitration register bit 24 (MARBR[24]) is changed from “Delayed Read Mode” to “PCI r2.1 Features Enable”. PCI 9054 Data Book sections 3.4.3.2 and 5.4.2.2, for M and C/J modes respectively, and the MARBR[24] register bit description, are revised as follows:

Table 4-35. (MARBR; PCI:08h or ACh, LOC: 88h or 12Ch) Mode/Arbitration Register

Bit	Description	Read	Write	Value after Reset
24	***PCI r2.1* Features Enable.** When set to 1, the PCI 9054 performs all PCI Read and Write transactions in compliance with *PCI r2.1*. Setting this bit enables Delayed Reads, 2^{15} PCI Clock timeout on Retries, 16- and 8-clock PCI latency rules, and enables the option to select PCI Read No Write Mode (Retries for writes) (bit [25]). Refer to Sections 3.4.3.2 and 5.4.2.2 for additional information. Value of 0 causes TRDY# to remain de-asserted on reads until Read data is available. If Read data is not available before the PCI Target Retry Delay Clocks counter (LBRD0[31:28]) expires, a PCI Retry is issued.	Yes	Yes	0

3.4.3.2 PCI r2.1 Features Enable

The PCI 9054 can be programmed through the PCI r2.1 Features Enable bit (MARBR[24]) to perform all PCI Read/Write transactions in compliance to PCI r2.1 (and PCI r2.2). The following PCI 9054 behavior occurs when MARBR[24] = 1.

3.4.3.2.1 Direct Slave Delayed Read Mode

PCI Bus single cycle aligned or unaligned 32-bit Direct Slave Read transactions always result in a 1-Lword single cycle transfer on the Local Bus, with corresponding Local Address and TSIZ[0:1] asserted to reflect the PCI Byte Enables (C/BE[3:0]#), unless the PCI Read No Flush Mode bit is enabled (MARBR[28] = 1) (refer to Section 3.4.3.3). This causes the PCI 9054 to Retry all PCI Bus Read requests that follow, until the original PCI Address and Byte Enables (C/BE[3:0]#) are matched.

3.4.3.2.2 2^{15} PCI Clock Timeout

If a PCI Master does not complete its originally requested Direct Slave Delayed Read transfer, the PCI 9054 flushes the Direct Slave Read FIFO after 2^{15} PCI clocks and will grant an access to a new Direct Slave Read access. The PCI 9054 Retries all other Direct Slave Read accesses that occur before the 2^{15} PCI clock timeout.

3.4.3.2.3 PCI r2.1 16- and 8- clock rule

The PCI 9054 guarantees that if the first Direct Slave Write data cannot be accepted by the PCI 9054 and/or the first Direct Slave Read data cannot be returned by the PCI 9054 within 16 PCI clocks from the beginning of the Direct Slave cycle (FRAME# asserted), the PCI 9054 issues a Retry (STOP# asserted) to the PCI Bus.

During successful Direct Slave Read and/or Direct Slave Write accesses, the subsequent data after the first access is accepted for writes or returned for reads in 8 PCI clocks (TRDY# asserted). Otherwise, the PCI 9054 issues a PCI disconnect (STOP# asserted) to the PCI Master.

In addition, setting the PCI r2.1 Features Enable bit (MARBR[24] = 1) allows optional enabling of the following PCI r2.1 function:

- No write while delayed read is pending (PCI Retries for writes) (MARBR[25])

The following PCI 2.1 optional function can be activated except if MARBR[25,24] = 11b:

- Write and flush pending delayed read (MARBR[26])

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PCI Bus single cycle aligned or unaligned 32-bit Direct Slave Read transactions always result in a 1-Lword single cycle transfer on the Local Bus, with corresponding Local Address and Byte Enables (LBE[3:0]#) asserted to reflect the PCI Byte Enables (C/BE[3:0]#), unless the PCI Read No Flush Mode bit is enabled (MARBR[28] = 1) (refer to Section 5.4.2.3). This causes the PCI 9054 to Retry all PCI Bus Read requests that follow, until the original PCI Address and Byte Enables (C/BE[3:0]#) are matched.

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4. EEPROM Serial Read Feature (CNTRL[27])

The information from the previously published design note is now included in the PCI 9054 Data Book rev. 2.1 sections 2.4.2 for M-mode and 4.4.2 for C/J modes.

5. BDIP# Pin

Feature Description: PCI 9054 revisions AB and AC support the BDIP# signal for continuous bursts (greater than four Lwords) differently than the MPC 850/860 4-Lword protocol. Whenever the Bterm and Burst functions are enabled for PCI Target and/or DMA transactions, or whenever Slow Terminate mode is enabled for DMA (DMAMODEx[15] = 0), the PCI 9054 will drive the BDIP# signal high until the last data transfer of the burst begins. On the last data transfer, the

PCI 9054 asserts BDIP# low indicating the last transfer of the burst transaction. BDIP# will be driven low for as long as that data is valid on the bus and will be negated on the following clock along with the BURST# signal.

6. Operation of PCI 9054 Buffers in 3.3 Volt Signaling Environment

The PCI 9054 has universal buffers that were designed to operate in either a 5 Volt or 3.3 Volt signaling environment. The PCI 9054 has a 3.3 Volt core and the I/O buffers are 5 Volt tolerant.

The PCI 2.2 specification specifies clamp diodes to both ground and VCC when operating in 3.3 Volt signaling environment. In the 5 Volt signaling environment, the high clamp diode is optional. The purpose of the clamp diodes is to ensure the reliability and signal integrity of the receiving devices when there are excessive voltage transients on the bus and to improve PCI bus signal integrity.

The PCI 9054 buffers have a clamp diode to ground, but no diode to VCC. Based on reliability and signal integrity evaluations, the PCI 9054 will operate properly in both 5 Volt and 3.3 Volt signaling environments in likely circuit configurations even though it does not have a high clamp diode. Some of the results of circuit simulations are described below. If the PCI 9054 is to be used in a configuration that exceeds the conditions of these simulations, please contact PLX.

- The PCI 9054 buffers are not susceptible to damage from input signal voltage transients called out by the specification (up to 7.1 Volts). In fact, the PCI 9054 can operate reliably in 5 Volt signaling environments with no high clamp diode protection, which means it withstands voltage spikes as high as 11 Volts.

- The response of the PCI 9054's PCI input buffers were simulated under various extreme configurations. For example with a 12" PCI trace length, 90 Ohms bus impedance, 0 degrees Celcius, 3.6 Volts and being driven by a strong output buffer (the PCI 9054's output buffer which has 35 Ohm output impedance) the PCI 9054 correctly interpreted the distorted digital waveform into the correct ideal digital waveform. Graphs of this and other waveforms are available from your local Area Sales Managers or FAEs.

Therefore, if the PCI 9054 is part of a 3.3 Volt circuit that connects to other PCI devices, it will properly interpret distorted signals. If there are non-9054 devices on the PCI bus, they will also be able to interpret distorted signals properly if they contain high clamp diodes.

7. Local Parity Error Status Bit and Interrupt Assertion

This issue is now re-published as PCI 9054AB Erratum #21 and as PCI 9054AC Erratum #7.

8. Hot Swap Register Accesses from Local Bus (Applies to revision AB only; fixed in AC silicon)

Design Issue: The PCI 9054 Hot Swap register (HS_CSR) is writable from the Local bus.

Recommendation: Whenever accessing the Hot Swap register (HS_CSR) from the Local Bus, the ENUM# status bit 7 value should be preserved, to avoid overwriting the bit prior to the PCI Hot Swap software acknowledging the current status.

9. Retried Direct Slave Single Read completed as Burst Read

Design Issue: If a Direct Slave Single Read request that has been retried by the PCI 9054 is completed as a Burst Read transaction, the PCI 9054 will stall the PCI bus with continuous retries on the second read data. If the PCI r2.1 Features Enable bit is set (MARBR[24] = 1), the PCI 9054 will issue a Target Abort following expiration of 32K PCI clock timeout. If this bit is clear (MARBR[24] = 0), the 32K PCI clock discard timer is not enabled.

The PCI Specification does not allow a PCI master to extend a read transaction beyond its original intended length after it has been terminated with Retry. Accordingly, the scenario described above can only occur if a second PCI master requests the same transaction (address, command, byte enables and parity) that is being retried for the original PCI master request. The PCI 9054 cannot and need not distinguish between the two and will simply attempt to complete the access.

Solutions/Workarounds: To avoid stalling the PCI bus under this scenario:

1. Set the PCI r2.1 Features Enable bit (MARBR[24] = 1) to enable 32K PCI clock timeout for retries.
2. Enable both the Read Ahead Mode feature (MARBR[28] = 1) and local Prefetch (LBRD0[8] = 0 for Space 0, LBRD1[9] = 0 for Space 1, and/or LBRD0[9] = 0 for Expansion ROM). This will allow the PCI 9054 to keep the read data in the FIFO and transfer it on the PCI request.

   This workaround is only applicable to memory-mapped address spaces. Although burst I/O transactions are legal in PCI, processors typically do not perform burst I/O and x86 processors cannot. Additionally the PCI

9054 will disconnect with the first data of a PCI I/O transaction. The PCI 9054 does not prefetch I/O-mapped address spaces, and therefore Read Ahead mode is not applicable to I/O-mapped spaces.

3. Limit the number of retries allowed from the PCI 9054 before discarding an uncompleted transaction and reporting retry timeout error.

10. Multiplexed output pin DMPAF (Direct Master Programmable Almost Full) negation or MDREQ# (M-Mode IDMA Request) assertion timing

Specification Clarification: In C-mode (non-multiplexed address and data) and J-mode (multiplexed address and data), the multiplexed pin DMPAF/EOT# is configured for DMPAF output functionality if EOT# functionality is disabled by clearing the DMAMODE0[14] and DMAMODE1[14] register bits (default configuration).

In M-mode (MODE0 and MODE1 pins high), the multiplexed pin MDREQ#/ DMPAF/EOT# is configured for MDREQ#/DMPAF output functionality if EOT# functionality is disabled by clearing the DMAMODE0[14] and DMAMODE1[14] register bits (default configuration). If M-mode MDREQ#/DMPAF output functionality is selected, the MDREQ# designation is applicable if this pin is used to signal a CPU IDMA data transfer request, and the DMPAF designation is used if this pin is used to signal that the Direct Master Write FIFO is almost full. DMPAF pin output assertion relies on the programmable value in DMPBAM[10, 8:5] to determine when to signal that the Direct Master Write FIFO is almost full. After DMPAF assertion, the PCI 9054 negates the DMPAF pin upon the last word of the transfer entering into the Data Out Holding Register. The DMPAF signal indicates the Direct Master Write FIFO status, not the completion of the transfer status.

In M-mode, MDREQ# output is normally always asserted, indicating local processor IDMA data transfer should start. MDREQ# negation relies on the programmable value in DMPBAM[10, 8:5] to determine when to signal that the Direct Master Write FIFO is almost full and to remove the IDMA request. After MDREQ# negation, the PCI 9054 asserts the MDREQ# pin upon the last word of the transfer entering into the Data Out Holding Register. The DMPAF signal indicates the Direct Master Write FIFO status, not the completion of the transfer status.

11. EEDI/EEDO pull-up/pull-down documentation

Design Issue: A pull-up or pull-down resistor is required on the EEDI/EEDO pin.

Recommendation: The Pin Description page of the Data Book (page 12-1) states that all I/O pins should have a pull-up or pull-down resistor. Page 12-1 should additionally refer to Tables 2-19 and 4-19. The following information replaces Tables 2-19 and 4-19 in the PCI 9054 Data Book.

Serial EEPROM Guidelines

Local Processor	Serial EEPROM	System Boot Condition
None	None	The PCI 9054 uses default register values and sets the Local Init Status bit (LMISC[2]). The EEDI/EEDO pin must be **pulled low** (rather than pulled high, as is typically done for this pin). A 1K Ohm pull-down resistor is required, which during initialization will cause the PCI 9054 to interpret that it has detected an EEPROM Start bit and zero values for EEPROM data. If the PCI 9054 detects an EEPROM Start bit and the first 33 bits of EEPROM data are all zeros, the PCI 9054 reverts to default register values and sets the Local Init Status bit (LMISC[2]).
None	Programmed	Boot with serial EEPROM values. The Local Init Status bit (LMISC[2]) must be set by the serial EEPROM. Responses to Direct Slave and PCI Configuration Space accesses are retries until initialization is complete. A pull-up resistor is required.
None	Blank	The PCI 9054 detects a blank EEPROM, reverts to default register values, and sets the Local Init Status bit (LMISC[2]). A pull-up resistor is required. If the PCI 9054 receives an EEPROM Start bit and the first 33 bits of EEPROM data are all 1's, the PCI 9054 presumes the EEPROM is blank, terminates further reading of the EEPROM data, and sets the Local Init Status bit (LMISC[2]).
Present	None	The Local processor programs the PCI 9054 registers, and then sets the Local Init Status bit (LMISC[2] = 1) when initialization is complete. Responses to Direct Slave and PCI Configuration Space accesses are retries until initialization is complete. A pull-up resistor is required. ***Note:*** *Some systems may hang if Direct Slave reads and writes take overly long (during initialization, the PCI Host performs Direct Slave accesses). Increasing the value of the Direct Slave Retry Delay Clocks (LBRD0[31:28]) may resolve this.*
Present	Programmed	Load PCI 9054 registers from the serial EEPROM, but the Local processor can reprogram the PCI 9054. Either the Local processor or the serial EEPROM must set the Local Init Status bit (LMISC[2] = 1). A pull-up resistor is required.
Present	Blank	The PCI 9054 detects a blank EEPROM, reverts to default register values, and sets the Local Init Status bit (LMISC[2]). A pull-up resistor is required. If the PCI 9054 receives an EEPROM Start bit and the first 33 bits of EEPROM data are all 1's, the PCI 9054 presumes the EEPROM is blank, terminates further reading of the EEPROM data, and sets the Local Init Status bit (LMISC[2]). ***Note:*** *In some systems, the Local processor may be too late to reconfigure the PCI 9054 registers before the BIOS configures them. The serial EEPROM can be programmed through the PCI 9054 after the system boots in this condition.*

Note: If the serial EEPROM is missing and a Local Processor is present with blank Flash, the condition None/None (as seen in the Table) applies, until the Processor's Flash is programmed.

All the above EEPROM configurations, with the exception of the None/None condition, require a 1K to 10K ohm (typically 4.7K) pull-up on the EEDI/DO pin.

12. PCI 9054 will occasionally drive LSERR# output in Test mode (applies to revision AB only; fixed in AC silicon)

Design Issue: The PCI 9054AB will occasionally drive the LSERR# output active (low) when the TEST pin is pulled high (for NANDTREE testing and/or for entering reduced power state), rather than floating the LSERR# output.

Recommendations: (use either or both)

1. Disable LSERR# output by configuring INTCSR[0] to the default value of 0, prior to driving the TEST pin high.
2. Three-state the LSERR# output from the PCI 9054AB through an external three-state buffer such as a 74xx125 (quad buffer), using the TEST input signal for the buffer Output Enable input.

13. PCI Target Abort during DMA Transfer

Design Issue: During a PCI-to-Local DMA transfer, if a Target Abort occurs on the last DMA data transfer cycle, the PCI 9054 will generate an unknown data cycle for the last data to the Local bus. A PCI Target Abort at any other time during the DMA transaction will be successfully completed. This is a rare case condition. If a Target Abort during a DMA transaction occurs, the system should repeat the operation.

Recommendation: A Target Abort is by definition an error condition, and if a Target Abort occurs the last data should be assumed to be invalid. After a DMA transaction is complete, software should check the Received Target Abort status bit (PCISR[12]). If the bit indicates that a PCI Target Abort occurred, software should repeat the DMA transaction.

14. Interrupt Control/Status register (INTCSR) indication of a Master Abort or Target Abort condition

Design Issue: When a Master Abort or Target Abort condition is detected, status bits INTCSR[27:24] reflect the most recent error condition depending on the abort received. Clearing the abort condition will not reset these status bits to their default values of 1.

Recommendation: The INTCSR[27:24] status bits indicating that a Master Abort or Target Abort was signaled or detected are updated when either another abort condition occurs, or a PCI reset is applied to the PCI 9054 (a software reset via CNTRL[30] will not change INTCSR register contents). Otherwise, these bits reflect the status of the last abort condition received. If monitoring of these bits is necessary for error recovery, monitor the equivalent PCI configuration register

error bits in the PCI Status register (PCISR[13:11]). PCI 9054 issuance of a Master Abort is signaled in PCISR[13], PCI 9054 issuance of a Target Abort is signaled in PCISR[11], and receipt of a Target Abort from another device while PCI 9054 is master is signaled in PCISR[12].

15. Power Management Interface Specification version support

Design Issue: The PCI 9054 Data Book indicates compliance with the PCI Power Management Interface Specification revision 1.1, however the PMC register description is compliant with revision 1.0. The PCI 9054 can support either revision. The only differences between these revisions, with respect to PCI 9054 support, are the Version bits [2:0] value (programmable by local bus processor), and the descriptions for bits [8:6, 4] for which the values are read-only and return a value of 0 regardless of revision. The Version bits value (001b or 010b), which has no effect on PCI 9054 operation, is used by software to determine PMC register format.

Recommendation: PMC register descriptions for revisions 1.0 and 1.1 are listed below. If revision 1.1 rather than revision 1.0 is to be supported, program the PMC register (via local bus processor) with the Version value (010b) to overwrite the PMC register default value, by changing the 32-bit value at Local Bus offset 180h from 00014801h to 00024801h.

Register 11-27. (PMC; PCI:42h, LOC:182h) Power Management Capabilities
(PCI Power Mgmt. r1.0)

Bit	Description	Read	Write	Value after Reset
2:0	**Version.** The value 001 indicates compliance with *PCI Power Mgmt. r1.0*.	Yes	Local	001
3	**PCI Clock Required for PME# Signal.** When set to 1, indicates a function relies on PCI clock presence for PME# operation. The PCI 9054 does not require the PCI clock for PME#, so this bit should set to 0.	Yes	Local	0
4	**Auxiliary Power Source.** Because the PCI 9054 does not support PME# while in a D3cold state, this bit is always set to 0.	Yes	No	0
5	**Device-Specific Initialization (DSI).** When set to 1, the PCI 9054 requires special initialization following a transition to a D0 uninitialized state before a generic class device driver is able to use it.	Yes	Local	0
8:6	***Reserved.***	Yes	No	000
9	**D1_Support.** When set to 1, the PCI 9054 supports the D1 power state.	Yes	Local	0
10	**D2_Support.** When set to 1, the PCI 9054 supports the D2 power state.	Yes	Local	0
15:11	**PME Support.** Indicates power states in which the PCI 9054 may assert PME#. Values: XXXX1 = PME# can be asserted from D0 XXX1X = PME# can be asserted from D1 XX1XX = PME# can be asserted from D2 X1XXX = PME# can be asserted from D3hot XXXXX = PME# cannot be asserted from D3cold	Yes	[14:11]: Local [15]: No	00000

Register 11-27. (PMC; PCI:42h, LOC:182) Power Management Capabilities
(PCI Power Mgmt. r1.1)

Bit	Description	Read	Write	Value after Reset
2:0	**Version.** The default value 001 indicates compliance with *PCI Power Mgmt. r1.0.* To instead indicate PMC register format compliance with Revision 1.1, this value should be set to 010.	Yes	Local	001
3	**PCI Clock Required for PME# Signal.** When set to 1, indicates a function relies on PCI clock presence for PME# operation. The PCI 9054 does not require the PCI clock for PME#, so this bit should set to 0.	Yes	Local	0
4	***Reserved.***	Yes	No	0
5	**Device-Specific Initialization (DSI).** When set to 1, the PCI 9054 requires special initialization following a transition to a D_0 uninitialized state before a generic class device driver is able to use it.	Yes	Local	0
8:6	**Aux_Current.** Supported by way of the PMDATA register per *PCI Power Mgmt. r1.1.*	Yes	No	000
9	**D_1_Support.** When set to 1, the PCI 9054 supports the D_1 power state.	Yes	Local	0
10	**D_2_Support.** When set to 1, the PCI 9054 supports the D2 power state.	Yes	Local	0
15:11	**PME Support.** Indicates power states in which the PCI 9054 may assert PME#. Values: XXXX1 = PME# can be asserted from D_0 XXX1X = PME# can be asserted from D_1 XX1XX = PME# can be asserted from D_2 X1XXX = PME# can be asserted from D_{3hot} XXXXX = PME# cannot be asserted from D_{3cold}	Yes	[14:11]: Local [15]: No	00000

16. Capability Pointers values must be either default value or 0

Design Issue: PCI 9054 default register values enable the Power Management, Hot Swap, and VPD Capabilities, defined by the PCI Bus Power Management Interface Specification, PICMG Hot Swap Specification, and PCI Local Bus Specification, respectively. PCISR[4] = 1 indicates presence of the Capabilities List, and the CAP_PTR (offset 34h) value (40h) acts as a pointer to the first Capability (Power Management) within this linked list. PCISR[4] and CAP_PTR are programmable from the Local bus only. The only valid values for CAP_PTR are the default value 40h, or 0h. If any Capabilities are enabled, the Power Management Capability must be enabled, with CAP_PTR containing the default value 40h to point to the Power Management Capability.

Each of the Power Management, Hot Swap, and VPD Capability register sets include a Next Capability Pointer register, in which the value acts as a pointer to the next Capability within the linked list. With default register values:

- PMNEXT (offset 41h) value (48h) points to the Hot Swap Capability registers,
- HS_NEXT (offset 49h) value (4Ch) points to the VPD Capability registers, and
- PVPD_NEXT (offset 4Dh) value (0h) indicates end-of-list (no additional Capabilities).

The only valid values for these Next Capability Pointer registers are the register's default value, or 0h to indicate end-of-list. These registers are programmable from the Local bus only, except for HS_NEXT which is additionally programmable from the serial EEPROM.

Recommendations:

1. The Hot Swap Capability can be selectively disabled by:
   - setting its ID in HS_CNTL (offset 48h) to 0h (programmable by Local bus or EEPROM).

2. The VPD Capability can be selectively disabled by:
   - setting its ID in PVPDCNTL (offset 4Ch) to 0h (writable (but not readable) from the Local bus), and/or
   - clearing HS_NEXT (offset 49h, programmable by Local bus or serial EEPROM).

3. Both Hot Swap and VPD Capabilities can be disabled by:
   - clearing HS_CNTL and HS_NEXT (programmable by Local bus or EEPROM), and/or
   - clearing PMNEXT(offset 41h, programmable by Local bus), and/or
   - setting both IDs (HS_CNTL and PVPDCNTL) to 0h.

Notes:

1. When writing HS_CNTL or HS_NEXT from the Local bus, the HS_CSR[7] ENUM# status bit must be preserved for revision AB silicon (fixed in revision AC).
2. PVPDCNTRL is writable but not readable from the Local bus.

17. Direct Slave Transfer Size

Issue: In PCI 9054 Data Book version 2.1, Table 3-3 lists how data is transferred onto the M-mode Local Bus during Direct Slaves Writes. The table is incorrect and is replaced by the Table 3-3 shown below.

Table 3-3. Data Bus TSIZ[0:1] Contents for Single Write Cycles

Transfer Size	TSIZ [0:1]		Address		32-Bit Port Size				16-Bit Port Size		8-Bit Port Size
			LA30	LA31	LD[0:7]	LD[8:15]	LD[16:23]	LD[24:31]	LD[0:7]	LD[8:15]	LD[0:7]
Byte	0	1	0	0	OP0	—	—	—	OP0	—	OP0
	0	1	0	1	—	OP1	—	—	—	OP1	OP1
	0	1	1	0	—	—	OP2	—	OP2	—	OP2
	0	1	1	1	—	—	—	OP3	—	OP3	OP3
Word	1	0	0	0	OP0	OP1	—	—	OP0	OP1	—
	1	0	1	0	—	—	OP2	OP3	OP2	OP3	—
Lword	0	0	0	0	OP0	OP1	OP2	OP3	—	—	—

Note: The "—" symbol indicates that a valid byte is not required during that Write Cycle. However, the PCI 9054 drives these byte lanes, although the data is not used.

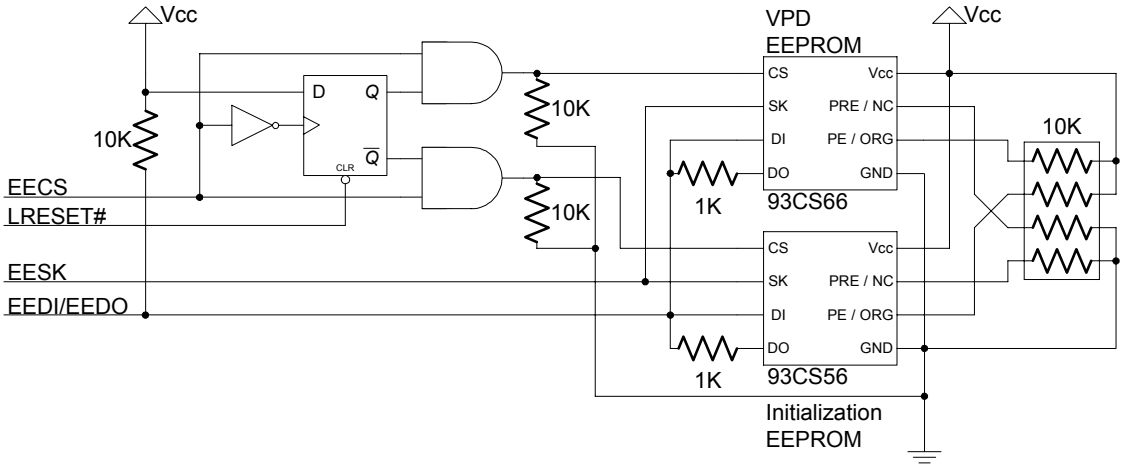
18. VPD Implementation

Documented Behavior: The PCI 9054 supports the Vital Product Data (VPD) optional feature detailed in PCI Specification r2.2. The PCI 9054 VPD feature supports storage of a VPD data structure within a serial EEPROM (2k- or 4k-bit, 3-wire interface). The PCI Specification defines the first element within this data structure as the Identifier String at VPD address 0h. Additionally, the PCI Specification requires that the VPD registers (in PCI Configuration Space) be used to read/write VPD data only.

At power-up reset, the PCI 9054 reads 88 bytes of configuration data from a serial EEPROM, beginning with the PCI Vendor ID value stored at address 0h. Although this address seemingly conflicts with VPD requirements, PLX choose to store configuration data beginning at address 0, in order to maintain compatibility with legacy devices (such as PCI 9080). Additionally, the PCI 9054 provides CNTRL[27:24] register bits to allow programming of configuration data within the serial EEPROM, without using the VPD registers.

Solution/Workaround: VPD data storage can be implemented with a serial EEPROM used exclusively for VPD (and not containing PCI 9054 configuration data). Because the PCI 9054 will attempt to read configuration data through the serial EEPROM interface at power-up reset, the VPD EEPROM should not be enabled until PCI 9054 initialization completes (when EECS de-asserts).

The following sample circuit includes two serial EEPROMs, one for initialization and the other for VPD, with only one EEPROM enabled at any time. The circuit initially enables the Initialization EEPROM during power-up reset. After the first EECS de-assertion, the circuit enables access to the VPD EEPROM and disables access to the Initialization EEPROM. The D flip-flop and inverter can both be replaced by a negative edge-triggered J-K flip-flop such as the 74HCT107, with its J input tied high and its K input tied low.

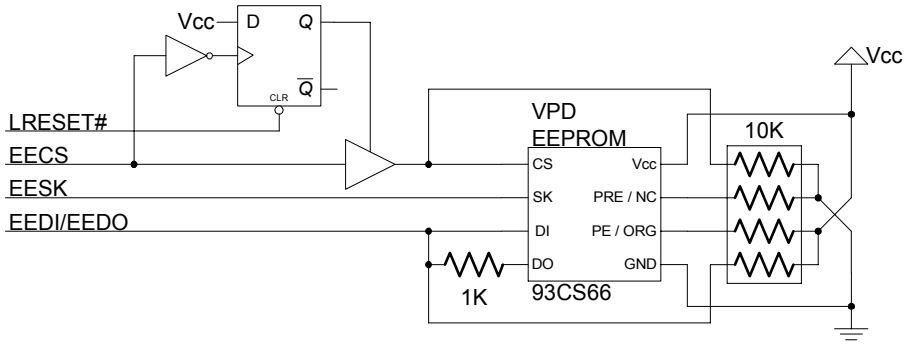


Sample VPD Implementation Circuit

To allow programming of the Initialization EEPROM, the circuit can be modified such that the flip-flop CLR input is driven by the output of an AND gate instead of from LRESET# directly, with LRESET# connected to one of the AND gate inputs. If any AND gate input is low, the gate output is low, which will enable the Initialization EEPROM and disable the VPD EEPROM.

The following sample circuit includes one serial EEPROM for VPD-only access, and applies to designs having a Local Bus processor that will initialize the PCI 9054, including setting of the Init Done bit (LMISC[2] = 1).

Sample VPD implementation circuit without initialization EEPROM, and Local CPU sets PCI 9054 Init Done bit



If neither a serial initialization EEPROM nor Local CPU is present to set the Init Done bit, the EEDI/EEDO line must be pulled low with a 1K resistor (which will cause the PCI 9054 itself to set the Init Done bit). To implement VPD in such case, the EEDI/EEDO line in the above circuit would have to be switched to connect only to a pull-down (removing connection to the EEPROM) during the time that the *Q* output of the D flip-flop is low.

The PCI 9054 will reload its configuration registers from serial EEPROM if the Reload Configuration Registers register bit (CNTRL[29]) is transitioned from 0 to 1, or when its Power State (PMCSR[1:0]) is transitioned from D3hot to D0 state. Transitioning the Power State from D3hot to D0 state causes LRESET# assertion, and therefore the circuit will correctly access the Initialization EEPROM in such case. Prior to any setting of the Reload Configuration Registers bit (CNTRL[29]), the designer should ensure that Initialization EEPROM access is enabled, by first performing a Software Reset (CNTRL[30]) to cause LRESET# assertion, since PCI 9054 registers must be reloaded with configuration data and not VPD data.